REMARKS

Applicants affirm the provisional election to prosecute the group I claims 1-32 and 59-71. Claims 18-19, 23-24, and 62-63 have been canceled. Thus, claims 1-17, 20-22, 25-32, 59-61, and 64-71 are pending in the present application.

In the Office Action, claims 5 and 18-19 was rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 18-19 have been canceled, rendering the Examiner's rejections of these claims moot. Claim 5 has been amended to correct a typographical error and thereby provide antecedent basis for "the device." Claim 5 has in no way been narrowed by virtue of this amendment and so this amendment should not be interpreted as narrowing the claimed invention for purposes of any determination under the doctrine of equivalents. Applicants respectfully request that the Examiner's rejections of claim 5 under 35 U.S.C. § 112, second paragraph, be withdrawn.

In the Office Action, claims 1-3, 20-22, 26, 50 9-61, and 65 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Brant, et al (U.S. Patent No. 5,848,435). Claims 4, 6-17, 27-32, and 66-71 were rejected under 35 U.S.C. 103(a) as being unpatentable over Brant in view of Baird, et al (U.S. Patent No. 6,732,278). Claims 5, 25, and 64 were rejected under 35 U.S.C. 103(a) as being unpatentable over Brant in view of Baird and further in view of Brock, et al (U.S. Patent No. 6,662,251). Claims 18-19, 23-24, and 62-63 were rejected under 35 U.S.C. 103(a) as being unpatentable over Brant in view of Hubis, et al (U.S. Patent No. 6,343,324). Claims 18-19, 23-24, and 62-63 have been canceled rendering the Examiner's rejections of these claims moot. The Examiner's remaining rejections are respectfully traversed.

Claims 1, 20, and 59 set forth a crypto-processor. As defined in the specification, a crypto-processor is a processor that performs cryptographic operations. In one embodiment, the crypto-processor is a specialized processor that includes specialized cryptographic hardware. In another embodiment, the crypto-processor includes a general-purpose processor programmed with cryptographic firmware or software. In still another embodiment, the crypto-processor includes a general-purpose processor modified with specialized cryptographic hardware. See Patent Application, page 31, ll. 21-25. Claim 1 also sets forth, among other things, a memory coupled to receive memory transactions through the crypto-processor, wherein the memory transactions are passed to the memory by the crypto-processor. Claims 20 and 59 set forth, among other things, receiving a request for a memory transaction at a crypto-processor and passing the request for the memory transaction to a storage device if the memory transaction is authorized for the storage location.

In contrast, Brant describes an address protection circuit that may compare a source identification code and a current bus address to a range of addresses stored in a content-addressable memory table. The address protection circuit may then control access to a memory based upon the comparison. See Brant, col. 3, line 62 – col. 4, line 32. However, Brant does not describe or suggest a cryptographic processor. For at least this reason, Applicants respectfully submit that the present invention is not anticipated by Brant and request that the Examiner's rejections of claims 1-3, 20-22, 26, 59-61, and 65 under 35 U.S.C. 102(b) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the prior art of record. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Brant is completely silent with

regard to a crypto-processor. Moreover, Brant fails to teach or suggest a memory coupled to receive memory transactions through the crypto-processor, wherein the memory transactions are passed to the memory by the crypto-processor, as set forth in claim 1. Brant also fails to teach or suggest receiving a request for a memory transaction at a crypto-processor and passing the request for the memory transaction to a storage device if the memory transaction is authorized for the storage location, as set forth in claims 20 and 59.

In rejecting Claims 4, 6-17, 27-32, and 66-71, the Examiner alleges that Baird describes a device different from a crypto-processor, wherein the device is configured to request memory transactions passed to a memory by the crypto-processor. Applicants respectfully disagree. Baird describes using a device 101 to access a site 105 via one or more potentially insecure devices in a network 106. The technique described by Baird may include providing a password to the site 105. However, Baird does not teach or suggest that the device 101 is configured to request memory transactions that are passed to a memory by a crypto-processor. In rejecting Claims 5, 25, and 64, the Examiner relies upon Brock to describe a bridge and first and second buses. However, Brock fails to remedy the aforementioned efficiencies in Brant and/or Baird.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not obvious over the prior art of record and request that the Examiner's rejections of claims 4-17, 25, 27-32, 64, and 66-71 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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